Matthew Song

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Education

Electrical Engineering and Computer Science B.S., *University of California, Berkeley* Graduated 2025

Relevant Coursework

Digital Design and ICs, Signals and Systems, User Interfaces, Prototyping and Fabrication, Operating Systems, Machine Structures, Machine Learning, Artificial Intelligence, Algorithms, Physics for Scientists and Engineers, Information Devices and Systems

Work Experience

SLAC National Accelerator Laboratory **August 2024 — Present**
Electrical Engineering and Programming Intern

- Resolved a critical, intermittent encoder issue in two weeks that had stumped two senior electrical engineers for over six months, ensuring beamline uptime
- Cloned and virtualized an outdated FPGA programming PC into a virtual machine, enabling continued support for legacy FPGAs
- Independently learned undocumented FPGA and PCB designs after a senior engineer retired, enabling rapid improvements to the control system that were critical for maintaining and improving beamline performance
- Engaged with component manufacturers to refine diagnostic approaches and improve motion control system reliability
- Analyzed PCB schematics using Altium to assess the capability of driving a detector trigger and provided actionable recommendations to optimize system performance
- Upgraded beamline FPGA hardware with high-reliability interlock logic critical to safe operation of expensive, sensitive instrumentation
- Designed and programmed an FPGA-based waveform generator to validate encoder performance under edge conditions

UAVs@Berkeley **Summer 2024 - Present**
President - previous Lead Electrical Engineer

- Led a multidisciplinary team to advance UAV design, including electronics, mechanical design, and control systems
- Designed and validated a custom PCB for a delayed-release payload controller
- Developed, debugged, and deployed firmware for the payload controller, ensuring robust performance during field testing
- Configured and debugged communication protocols including CAN, I2C, and UART for seamless on-board and off-board component interaction

Projects

FPGA RISC-V CPU **November — December 2024**

- Designed and implemented a 3-stage pipelined RISC-V CPU in Verilog on a Xilinx PYNQ-Z1 board
- Implemented synchronization, signal smoothing, and button parsing modules to allow interfacing with the real world
- Designed a UART communication module for streamlined communication between the CPU and external systems

FPGA Computer Vision Accelerator **March — April 2024**

- Designed, routed, and brought up a Zynq-7000 SoC PCB to accelerate the ORB computer vision algorithm for a UAV system
- Integrated DDR3, gigabit ethernet, and USB 2.0 interfaces, ensuring signal integrity with trace optimization and simulation
- Engineered the system for mechanical compatibility with the UAVs@Berkeley competition hexacopter

GPS-Denied UAV Navigation **November — December 2024**

- Developed a computer-vision-based geolocation system enabling UAV navigation in GPS-denied environments
- Set up and troubleshot RTSP video streams from the onboard camera system to the flight computer
- Evaluated and optimized image processing pipelines to enhance geolocation accuracy
- Conducted full-system test flights with in-field debugging and performance validation

Fully Custom 3D Printer **June 2024**

- Self-sourced and built a modified Voron 2.4 3D printer
- Designed and programmed an autonomous, reliable, dockable bed probe for consistent leveling
- Configured and compiled custom software and firmware on Raspberry Pi and STM32 platforms
- Tuned resonance and backlash compensation to achieve high-speed, precision prints

Skills

Altium, Xilinx Vivado, Python, Java, C/C++, Drones, Ardupilot, oscilloscope and multimeter usage, RISC-V, Git, Solidworks, 3D printing, SMD soldering